ABSTRACT OF THE DISCLOSURE

A ferroelectric memory device includes a plurality of bit line pairs, a plurality of sense amplifiers, a plurality of memory cells, a plurality of reference cells, and a control circuit. Each of the bit line pairs is composed of first and second bit lines. Each of the sense amplifiers amplifies a potential difference across the corresponding bit line pair. The memory cells are provided for the respective bit line pairs and each composed of a transistor and a ferroelectric capacitor. The reference cells are provided for the respective bit line pairs and each composed of a transistor and a ferroelectric capacitor. In addition, each of the reference cells on each of the bit line pairs retains data different from data of a reference cell on the adjacent bit line pair. The control circuit drives the sense amplifiers, the memory cells, and the reference cells. During the drive of the sense amplifier, the control circuit inactivates a reference word line connected to the reference cell.